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MARIANO OLMOS MARTÍN

RTL Desing/Verification Engineer

Electronic Engineer specialized in RTL design and verification, with experience in developing FPGA-based solutions and strong expertise in hardware description languages such as VHDL and SystemVerilog. Proficient in verification environments using UVM or OSVVM to ensure design quality and functionality.

EXPERIENCE

FPGA Engineer, *Indra* *[2024 – Present]·[Madrid,Spain]*

- Developed and optimized RTL (Register Transfer Level) in VHDL code for FPGA implementations, ensuring efficient and reliable hardware performance.
- Designed, simulated, and verified digital circuits using Sytemverilog wiht UVM,OSVVM ,Vivado and ISE tools to meet project specifications and requirements.
- Implemented complex algorithms and system functionalities in HDL for various FPGA applications.

OTHER

Speaker - FPGA Conference 2025, Germany, *Munich* *[2025]*

- Speaker at **FPGA Conference Europe 2025** (Munich, 1–3 Jul 2025): *"Mixed Verification: Regression Simulation Testbench with UVM for RTL Modules in VHDL."*
- Designed and implemented a **self-checking regression testbench** combining **VHDL (RTL)** with **SystemVerilog/UVM** (monitor/driver/scoreboard), improving coverage, debug speed, and RTL quality.

EDUCATION

Master's Degree in Microelectronic Design Engineering

[2025- 2027]·[Universidad Carlos III, Spain]

Degree in Communications Electronics Engineering

[2019 – 2024]·[Universidad de Alcalá, Spain]

LANGUAGES

- ✓ English (C1)
- ✓ Spanish(Native)

SKILLS

- ✓ VHDL , Verilog, SystemVerilog , HLS
- ✓ C, C++ , TCL , Python
- ✓ FPGAs, SoC, ASICs
- ✓ Risc-V , Microprocessors Microcontrollers , STM-32
- ✓ MATLAB
- ✓ DAC,ADC,DSPs
- ✓ UART, SPI, I2C
- ✓ Digital Control
- ✓ Hardware,PCB
- ✓ Linux
- ✓ Questa, Modelsim
- ✓ Xillinx , Zynq
- ✓ Verification , UVM
- ✓ OSVVM, UVVM
- ✓ Vivado
- ✓ GHDL